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Phenomenological model of grain boundary behaviour under a bias field in Nb-doped $CaCu_3Ti_4O_{12}$ ceramics

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ABSTRACT

In this work, the dielectric behaviour and capacitance–voltage (*C–V*) curves under an applied DC bias field of 1 wt% Nb-doped $CaCu_3Ti_4O_{12}$ ceramics have been studied. The dielectric properties reveal the existence of grain boundaries of different electrical nature. A new model is proposed to simultaneously explain the presence of insulating and conducting grain boundaries. At low frequency, the capacity curve of the material exhibits a double metal oxide semiconductor (MOS) capacitor-like behaviour and as the frequency is increased, the curve suffers an inversion showing a ferroelectric-like response. This behaviour does not correspond to ferroelectric domain movement phenomena but seems associated to charge accumulation on grain boundary regions.

1. Introduction

$CaCu_3Ti_4O_{12}$ (CCTO) ceramics are novel materials that recently have attracted much attention due to their unusual dielectric characteristics. CCTO possesses a giant dielectric constant of 10^5 [1] that presents good stability in a broad frequency (DC to 10^6 Hz) and temperature (100–400 K) range [2]. Besides its high permittivity, CCTO exhibits nonlinear current–voltage behaviour, attributed by some authors to Double Schottky Barriers (DSB) formed at the grain boundaries [3]. The origin of these behaviours is still controversial and many models have been proposed, having most of them in common the very important role of extrinsic mechanisms. The grain boundary layer capacitor mechanism based on the microstructure inhomogeneity and the formation of non-conductive grain boundaries between conductive grains, is one of the most accepted.

High dielectric constant values are usually associated to ferroelectric or relaxor materials and some authors [4,5] proposed that CCTO can be included in this category. According to Cillessen et al. [6] hysterestic behaviour could occur if there is a threshold field for charge transport across a certain interface layer, which is not ferroelectric. A ferroelectric-like hysteresis loop was obtained for a non ferroelectric system consisting of two Schottky contacts with a large concentration of traps distributed over a finite thickness near the electrodes [7].

The grain boundary plays the main role in the dielectric behaviour of ceramic CCTO. Its composition is not clear yet, but several studies propose that it is composed mainly of CuO and also that this composition could be modified during the sintering process [8]. CuO is a semiconductor with a band gap of about 1.4 eV, although band theory predicts it to be metallic; this discrepancy between experiments and theory has also been found for NiO and CoO [9]. Grain boundary effects have previously been studied in CCTO using a bias field. Liu et al. [10] found that low frequency DC-bias-field induced dielectric relaxation in the imaginary part of the dielectric permittivity, associated to electrode polarization and grain boundary response. Other authors have reported the nature of the low frequency plateau in the dielectric spectra, associating this relaxation to a hybrid response of grain boundaries and electrode contacts [11]. In order to explain the physical processes underlying this plateau, Fang and Chung [11] proposed a defect model based on previous works, in which the Cu ions located at the grain boundaries form acceptor states developing a potential barrier.

In this work the electrical behaviour of grain boundaries is studied and a phenomenological model is proposed to explain the low frequency dielectric relaxation. The study has been focus on Nb-doped CCTO, hereinafter CCTON, since we have previously demonstrated that this material shows higher dielectric constant values than CCTO together with nonlinear *I–V* characteristics [8].

2. Experimental procedure

Donor doped samples, with 1 wt% cations of Nb^{5+} substituting Ti^{4+} cations, $Ca_{0.25}Cu_{0.75}Ti_{0.99}O_{3.005}Nb_{0.01}$ (CCTON) ceramics were prepared using a solid state reaction and sintering process. The analytical grade $CaCO_3$ (Aldrich St. Louis, MO), TiO_2 (Merck Darmstadt, Germany), CuO (Aldrich St. Louis, MO) and Nb_2O_5 (Fluka) were mixed at the stoichiometric relation for 2 h, by attrition milling with 1.2 mm Zirconia balls, using de-ionized water as liquid medium and 0.2 wt% of Dolapix C64 (Zschimmer and Schwarz, Villareal, Spain) as dispersant. The milled powders were dried and sieved trough a 100 μm mesh, calcined at 900 °C for 12 h and then attrition milled again for 3 h. Organic binders (0.6 wt% of polyvinyl alcohol, PVA, and

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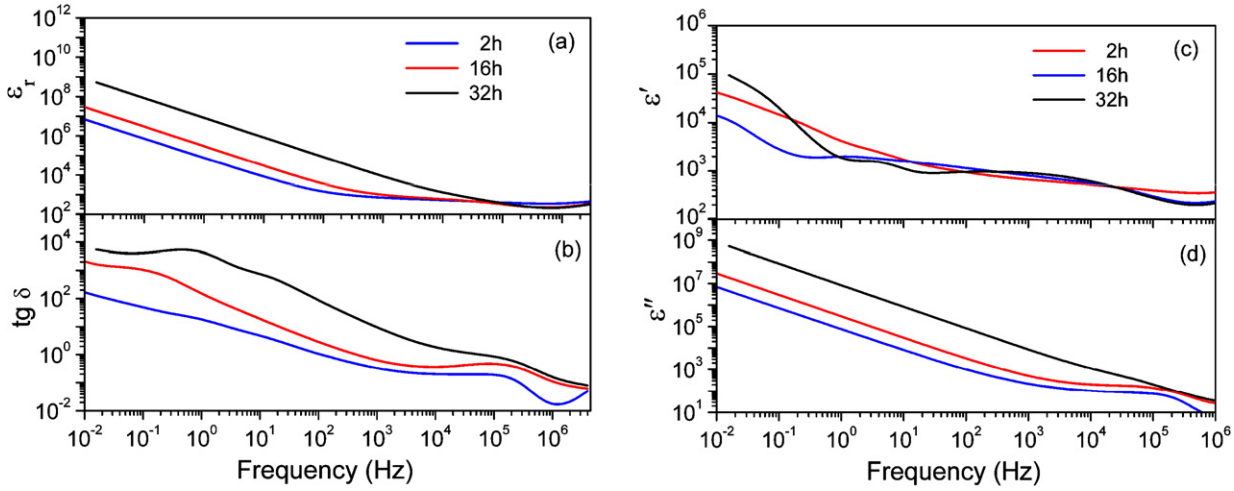

Fig. 1. Dielectric constant of CCTON ceramics sintered for 2, 16 and 32 h. (a) Relative dielectric constant, ε_r, (b) dielectric losses, $t_g\ \delta$, (c) real part of the dielectric constant, ε', and (d) imaginary part of the dielectric constant, ε''.

0.3 wt% of Polyethylene Glycol, PEG) were added into the calcined powders upon milling to help the formation of compacts. Powders were dried and sieved trough a 63 μm mesh and uniaxially pressed at 200 MPa into discs of 8 mm in diameter and 1.3 mm in thickness. The pellets were sintered in air at 1100 °C for 2, 16 and 32 h. All samples show a density over 95% of the theoretical density. The X-ray Diffraction analysis was performed on a Siemens Kristalloflex difractometer using Cu $K\alpha_1$ radiation and Ni filter. Polished discs were electroded with Ag sputtering (Bal-Tec SCD050) to form a parallel plate capacitor. The dielectric properties were measured at room temperature in the frequency range of 10^{-2} Hz–1 MHz, using an impedance analyzer (HP4294A, Agilent Technologies Inc. Santa Clara, CA). Under an applied DC bias field (±6 V) the C–V curves were evaluated in the range from 100 Hz to 10 MHz, using the same impedance analyzer.

3. Results and discussion

The dielectric behaviour of CCTON ceramics sintered for 2, 16 and 32 h, from 10^{-2} to 10^6 Hz, is shown in Fig. 1. Fig. 1(a and b) shows the relative dielectric constant and the dielectric losses values, respectively, and Fig. 1(c and d) the real, ε', and imaginary, ε'', parts of the dielectric constant associated to the capacitive and conductive phenomena. At all sintering times, both the dielectric constant and the dielectric losses decrease as the frequency increases. At low frequency, when the electrical response is governed by the grain boundary region, all dielectric parameters are greater and the dielectric constant exhibits a giant value. From 10^2 to 10^6 Hz, when the bulk dominates the electrical response, the dielectric parameters indicate a normal dielectric response. At low frequencies, 10^{-2} to 10^2 Hz, the relative dielectric constant exhibits the same trend than the imaginary part of the permittivity that it is related to the dielectric losses. At higher frequency values, 10^2 to 10^6 Hz, the permittivity trend becomes similar to the one exhibited by the real part of the dielectric constant, ε'. Therefore, the giant dielectric response of CCTO-like ceramics at low frequencies could be associated to conduction processes that occur in the grain boundary region.

CCTO is an electrically heterogeneous ceramic, commonly considered to consist of semiconducting grains and insulating grain boundaries [12] and in this context we studied the impedance behaviour of ceramic pellets sintered for 2–32 h. The data were analyzed using an equivalent circuit consisting of two RC parallel elements connected in series, one representing the semiconducting grains and the other one associated to the insulating grain boundary regions. Based on this equivalent circuit, CCTO exhibits two electroactive regions defined by two impedance semicircles: from the semicircle at lower frequencies the grain boundary R and C elements can be determined and from the higher frequencies one the bulk response. These values, detailed in Table 1, show that as the sintering time increases the resistance of both the bulk and the grain boundary regions diminishes. This behaviour is in accordance with the IBLC model for the bulk region but not for the grain boundary one, that would be expected to become more insulating as the permittivity rises up. Therefore, the dielectric constant is greater when the system is more semiconducting and the difference in conduction between grains and grain boundaries is lower, in disagreement with the IBLC model. The electrical characterization of the pellets suggests that the best dielectric constant values are obtained at long sintering times when grain boundaries are more conductive and the difference between bulk and grain boundaries conduction is small.

In addition the I–V curve of CCTON ceramics previously studied shown that the breakdown voltage diminished as the sintering time increases [8]. The number of active barriers can be estimated using a simple relation [13] that indicates the percentage of barriers that contribute to the rectification of the system i.e. Schottky-like barriers. Moreover the best permittivity values occur when the percentage of rectifying Schottky barriers diminishes.

Taking these results into account, it seems difficult to adjust and explain the dielectric behaviour of CCTON only considering an IBLC model, based in the idea of semiconducting grains and insulating grain boundaries. The results indicate that in some cases, the system acts as a conductive material and therefore a new model seems necessary to conciliate these two scenarios. We propose a new model, Fig. 2 that describes CCTO ceramics as n-type semiconductor grains [14] separated by a p-type semiconductor intergranular phase composed mainly of CuO. Φ_B, is the energy needed for the electronic carriers to overcome the intergranular barrier and jump from one grain to another. This barrier potential changes under an applied voltage in a way that depends on the relative resistances of grain (R_g) and grain boundary (R_{gb}). The two scenarios that this

Table 1
Capacitance (C) and resistance (R) values of bulk and grain boundary regions in CCTON ceramics sintered for different times.

Sintering time	Bulk		Grain boundary	
	R (Ω)	C (F)	R (Ω)	C (F)
2 h	–	–	1.24×10^7	6.06×10^{-10}
16 h	4.08×10^4	4.40×10^{-11}	1.02×10^5	4.99×10^{-10}
32 h	2.10×10^3	9.91×10^{-11}	1.99×10^4	4.52×10^{-10}

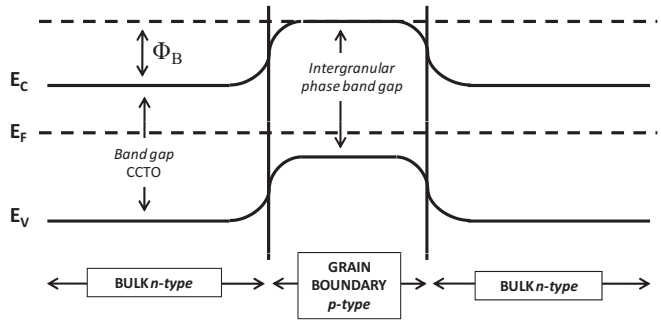

Fig. 2. Structure of grain boundary in CCTO-like ceramics, based in a n-p-n junction.

model considers are as follows:

$$R_{bg} >> R_g \rightarrow \Delta\Phi_B(V) < 0; \quad C(V) < 0;$$
$$\times \quad \text{Schottky Barrier-like behaviour} \qquad (1)$$

$$R_{bg} \sim R_g \rightarrow \Delta\Phi_B(V) > 0; \quad C(V) > 0; \quad \text{MOS-like behaviour} \qquad (2)$$

The first case (1) occurs when a voltage is applied and the barrier height diminishes due to the carrier accumulation on the semiconducting grain near to the grain boundary. At a certain voltage the carriers jump over the grain boundary to the next semiconducting grain. This charge transport produces a reduction of the capacitance with the applied field. The second scenario (2) takes place when the application of voltage induces an increase in the barrier height that raises capacitance. In this case, the charge carriers on both the grain and grain boundary phase accumulate at either side of the interphase, causing an increase in the barrier height ($\Delta\Phi_B(V) > 0$). At a certain voltage the carriers reach the grain boundary barrier and recombine with the intergranular phase carriers giving rise to conduction along the grain boundary phase, which shows smaller resistance. The observed increase in capacitance when applying a voltage is in agreement with Metal Oxide Semiconductor-like (MOS) behaviour.

These two scenarios are not exclusive; occurring simultaneously in the same sample and can be enhanced varying the processing conditions as observed in our samples. If a capacitor material is to be prepared, the grain boundary structure should behave as Schottky barrier, case (1), in accordance to the IBLC model, with a very high grain boundary resistance. This material shows low dielectric losses since conduction effects are not limited. As shown in Fig. 2, grain boundary conduction can occur at low frequencies. Scenario (2) should be very useful for applications as a sensor material. In this case, the conduction along grain boundaries would be very sensitive to small variations on their nature as those that can be produced by the presence of certain gases. Therefore, this model supports different new applications for CCTO ceramics depending on the main grain boundary structure. In Fig. 3, a sketch of the two possible scenarios of the n-p-n model is shown. Fig. 3(a) represents the ideal Schottky barrier and Fig. 3(b) the conduction along the grain boundary.

In order to corroborate the phenomenological model a set of electrical measurement under DC bias field were attempted on the 32 h CCTON ceramic sample. In Fig. 4(a) the capacitance under a bias field curves, from −6 to +6 V, at selected fixed frequencies, from 10^2 to 10^5 Hz, are shown. The DC bias field was swept in three steps: 0–6 V, 6 to −6 V and finally −6 to 0 V. The capacitance variation under a DC bias field is inversely proportional to the frequency and all curves are symmetrical to the zero bias field. As the frequency is increased the capacitance–voltage curve (*C*–*V* curve) suffers an inversion, corresponding to different behaviours at different frequency ranges. At low frequency values, 10^2–10^4 Hz, when grain boundary phenomena are relevant, the capacitance increases with the bias field. This behaviour of the *C*–*V* curve resembles the one of a low frequency double Metal Oxide Semiconductor capacitor, as both of them exhibit the same dependence of the capacitance under an applied bias field. The capacitance of the MOS structure depends on the voltage (bias) applied to the gate. There are roughly three regimes of operation [15]: (i) *Accumulation*, in which mobile carriers of the same type as the body accumulates at the surface (ii) *Depletion*, in which the surface is devoid of any mobile carriers leaving only a space or charge depletion layer and (iii) *Inversion*, in which mobile carriers of the opposite type to the body aggregate at the surface to "invert" the conductivity type. These three regimes are separated by two voltages: Flat band Voltage (V_{FB}) and Threshold Voltage (V_T).

From 0 to −5 V and from 0 to +5 V, the capacitance increases almost linearly due to charge accumulation of both grain and grain boundary carriers increasing the barrier height. From −5 to −6 V and from 5 to 6 V, the voltage is high enough to promote charge carriers into the grain boundary, the conduction suffers an inversion and the capacitance decreases.

At higher frequencies, when the bulk behaviour is more important, Fig. 4(c), the capacitance decreases with the bias field as would be expected for a dielectric material. It is also worth to notice that at low frequency, the capacitance dependence of the applied bias

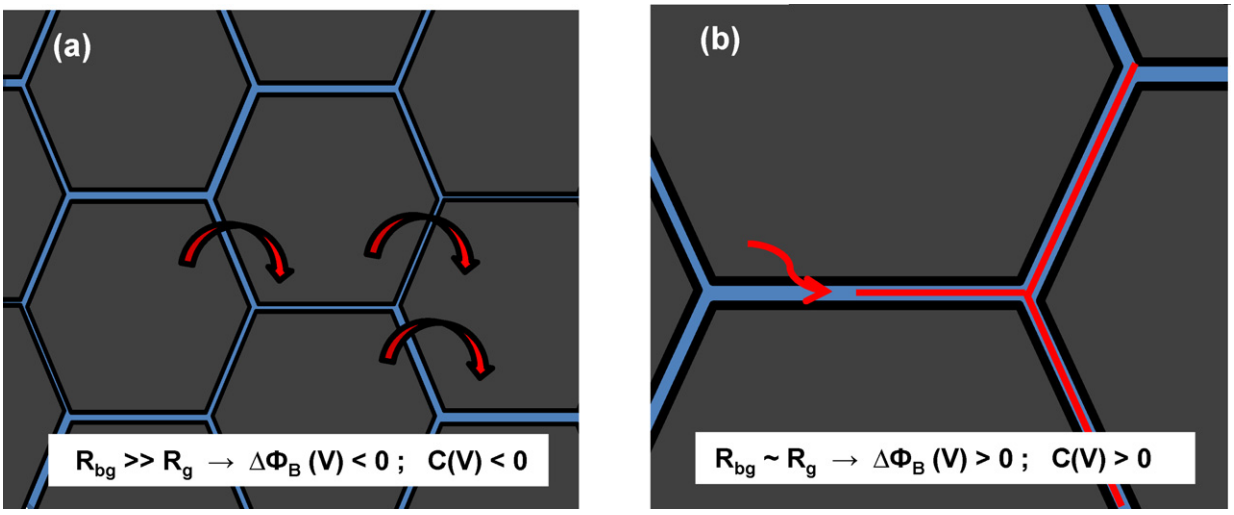

Fig. 3. Sketch of the two conduction mechanisms explained with the n-p-n model. (a) Conduction across a grain boundary. (b) Conduction along the intergranular phase.

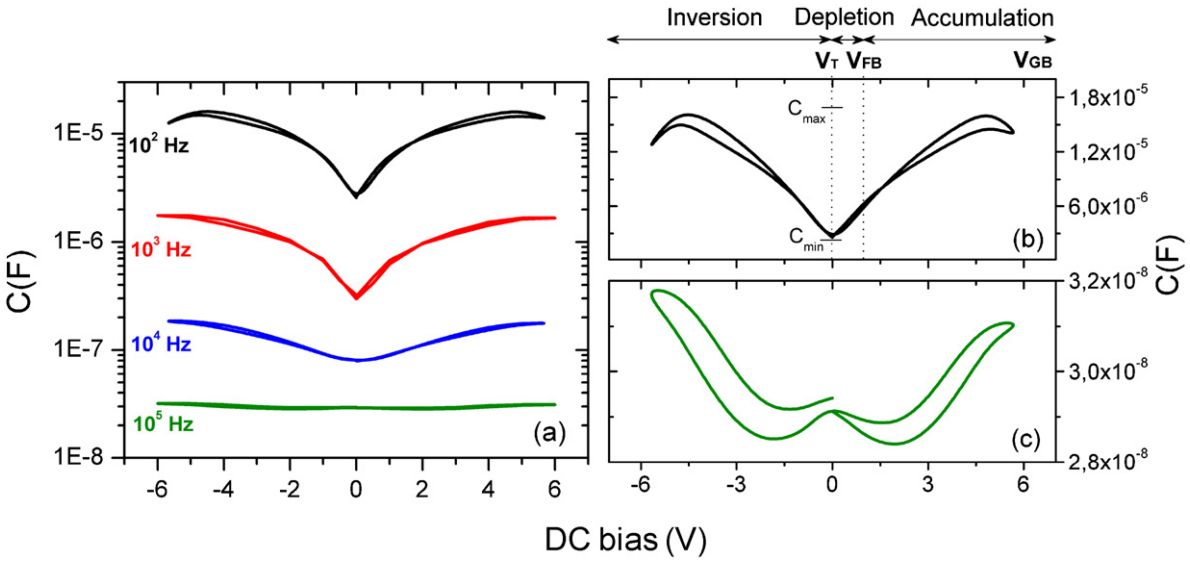

Fig. 4. DC bias field dependence of the capacitance at selected fixed frequencies (a) 10^2–10^5 Hz (b) 10^2 Hz (c) 10^5 Hz.

field is very strong but tends to decrease as the frequency increases being almost negligible at 10^5 Hz.

From the capacitance–voltage relationship it is possible to determine carrier density and flat band potential using the Mott–Schottky, MS, approximation for an n-type semiconductor:

$$\frac{1}{C_{SC}{}^2} = \frac{2}{eN_D\varepsilon\varepsilon_0}\left(V - V_{ES} - \frac{KT}{e}\right) \quad (3)$$

where ε is the dielectric constant of the sample, ε_0 is the vacuum permittivity (8.854×10^{-12} F/m) and e is the electric charge (1.602×10^{-19} C). V is the applied voltage, V_{FB} is the flat band potential, N_D is the donor density and C_{SC} is the space–charge capacitance. According to the MS approximation, when $1/C_{SC}{}^2$ is plotted vs V the slope of the linear plot will be $2/\varepsilon\varepsilon_0 eN_D$. When KT/e is negligible, the flat band potential can be obtained by extrapolating the linear portion of the plot to $1/C_{SC}{}^2 = 0$ [16]. Then, in this case, the flat band potential would be equivalent to the built-in potential in a p-n junction.

The Mott–Schottky approximation is only valid at low frequencies when the system is stable. In Fig. 5 the square capacity dependence on the bias field at 10^2 Hz is plotted. The linear region at low bias values, 0–0.5 V, meaning blocking of charge, can be adjusted to a straight line obtaining the donor density from the slope and the flat band potential from the intercept in the y axis.

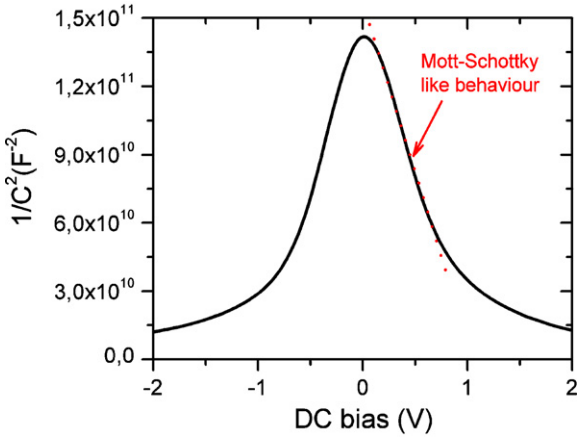

Fig. 5. DC bias field dependence of $1/C^2$ at 10^2 Hz.

The slope of the linear regime adjustment remains almost constant in the range 10^2–10^3 Hz. The extrapolated experimental values are $N_D = 4.90 \times 10^{20}$ m^{-3} and $V_{FB} = 0.77$ eV which are in good agreement with reported values for the barrier height [17].

The occurrence of a MOS-like behaviour seems to be related to the CuO-rich grain boundary phase and its semiconductor behaviour. The relevance of the present finding is related to the fact that the IBLC model usually proposed to explain CCTO ceramics, is worthy to explain its giant dielectric constant, but fails to provide routes for tailoring such properties by doping or processing [8,18–23] being the results not conclusive. Meanwhile the double Schottky barrier main contribution is to limit the charge transport up to the breakdown voltage, the double MOS capacitor approach implies that the nature of the secondary phase is of great relevance and governs the conduction along the grain boundary region.

The C–V curve behaviour can be expressed in terms of polarization response of the material. In Fig. 6 the polarization response under an applied bias field at selected fixed frequencies is shown. At low frequency, the system exhibits an antiferroelectric-like loop but at higher frequencies the behaviour is linear, with no evidence of ferroelectric or relaxor-like curves. The hysteretic behaviour of the curve at low frequency indicates an internal field responsible for the polarization. This behaviour does not correspond to

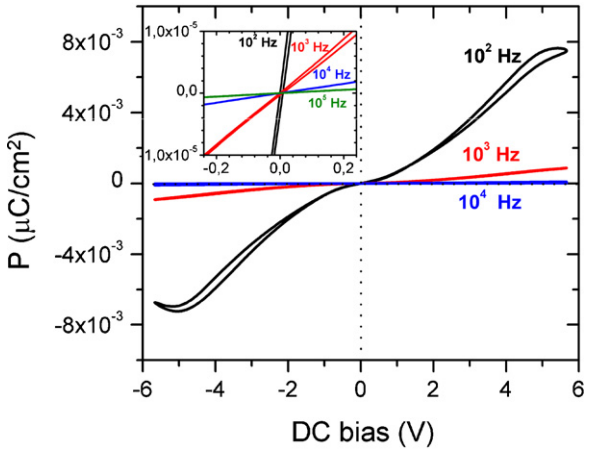

Fig. 6. DC bias field dependence of the polarization at selected fixed frequencies. Inset shows the polarization response at low bias values.

ferroelectric domain displacement phenomena but seems associated to charge accumulation on grain boundary regions.

4. Conclusions

In summary, CCTON electrical behaviour has been studied and the results reveal the existence of grain boundaries of different electrical nature, i.e. Schottky-like barriers and conductive ones. A phenomenological model of the grain boundary structure has been proposed. This model suggests that the giant dielectric constant is not intrinsic to the material but apparent and it is caused by conduction effects. To obtain real giant permittivity values, modification of grain boundaries is necessary in order to get Schottky-like barriers. High dielectric losses are associated to conduction effects and can be controlled modifying the grain boundary nature.

The capacitance–voltage (C–V) behaviour has been characterized at selected fixed frequencies applying forward and reverse bias field, revealing a strong dependence on the frequency. At low frequency, the material exhibits a Metal Oxide Semiconductor capacitor-like curve that turns into a ferroelectric-like loop as the frequency is increased.

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